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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,654	08/19/2003	Toshio Miyazawa	520.39294CX1	3745

20457 7590 06/15/2005

ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-3873

EXAMINER	
PARKER, KENNETH	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/642,654	MIYAZAWA ET AL.	
	Examiner	Art Unit	
	Kenneth A. Parker	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al 5933205 in view of Hasegawa 5064779, and further in view of Okumura et al 6391747 or Hara et al 5970369.

The primary reference shows regarding claim 3: A liquid crystal display device provided with a pixel area on a substrate having a plurality of gate lines (see figure 10 and other), a plurality of drain lines 350, a plurality of thin film transistors

(shown at the intersection and elsewhere)and a plurality of pixel electrodes P20 (shown in figures 13-14 and elsewhere) corresponding to said plurality of thin film transistors, and a drive circuit area disposed at a periphery of said substrate and having a drive circuit 352 and 364 (described at the bottom of column 10 and elsewhere) for driving said plurality of thin film transistors, said plurality of thin film transistors comprising: a polycrystalline silicon semiconductor layer 13 formed on said substrate 50, a gate electrode 9 formed on said polycrystalline silicon semiconductor layer with a gate insulating film (shown in figures 14b and 14c) interposed therebetween, an insulating film 65 to cover said polycrystalline silicon semiconductor layer, said gate insulating film and said gate electrode, a drain electrode 72 formed on said insulating film and electrically connected to said polycrystalline silicon semiconductor layer, and a source electrode 71 formed on said insulating film, spaced from said drain electrode and electrically connected to said polycrystalline silicon semiconductor layer. However the reference lacks the unevenness of a surface of said polycrystalline silicon semiconductor layer being within 10% of a thickness of said polycrystalline silicon semiconductor layer immediately after recrystallization with a laser.

The primary reference lacks regarding claim 4 the unevenness of said surface of said polycrystalline silicon semiconductor layer is present under said gate insulating film.

So the two missing element from the claims are the flatness of the layer and the evenness of the doping (the roughness under the gate electrode insulator is inherent

as no one gets the roughness down to zero). Regarding the smoothness, the secondary references indicate that keeping the surface smooth improves the device performance. Hasegawa indices that the surface should be smooth (as possible-abstract, and less than 10 angstroms in spec) and that that enables the ability to control doping depth (col. 6, lines 30-49).

Hara et al discloses a method of putting down two layers and recrystallizing with a laser, which should enable less then 10% roughness inherently. Hara teaches that this method enables putting down a good film at low energy (column 2). Therefore one of ordinary skill would have found motivation, teaching or suggestion to employ the recrystallization method of Hara, and would have found motivation to make the layer as smooth as possible and less than 10% for the benefits as taught by Hasagawa.

Okumura et al discloses a method of putting down a silicon layer with a cover and recrystallizing with a laser, which should enable less then 10% roughness inherently. Okumura teaches that this method enables putting down a film of superiour flattnes and a large grain size (column 3). Therefore one of ordinary skill would have found motivation, teaching or suggestion to employ the recrystallization method of Okumura, and would have found motivation to make the layer as smooth as possible and less than 10% for the benefits as taught by Hasagawa.

The smooth surface should enable better control of doping depth, but also Hasegawa indicates discusses it as desirable (in the connection with the discussion of giving even device properties it is described as an end goal). Therefore it would have

been inherent to the Yamazaki device as modified above, but also obvious to one of ordinary skill as the it was indicated as desirable.

Claims 1-2, 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al 5933205 in view of Hasegawa 5064779, in view of Takahashi et al 5712496, or Ipri 4597160.

The primary reference shows regarding claim 1: A liquid crystal display device provided with a pixel area on a substrate having a plurality of gate lines (see figure 10 and other), a plurality of drain lines 350, a plurality of thin film transistors (shown at the intersection and elsewhere)and a plurality of pixel electrodes P20 (shown in figures 13-14 and elsewhere) corresponding to said plurality of thin film transistors, and a drive circuit area disposed at a periphery of said substrate and having a drive circuit 352 and 364 (described at the bottom of column 10 and elsewhere) for driving said plurality of thin film transistors, said plurality of thin film transistors comprising: a polycrystalline silicon semiconductor layer 13 formed on said substrate 50, a gate electrode 9 formed on said polycrystalline silicon semiconductor layer with a gate insulating film (shown in figures 14b and 14c) interposed therebetween, an insulating film 65 to cover said polycrystalline silicon semiconductor layer, said gate insulating film and said gate electrode, a drain electrode 72 formed on said insulating film and electrically connected to said polycrystalline silicon semiconductor layer, and a source electrode 71 formed on said insulating film, spaced from said drain electrode and electrically connected to said polycrystalline silicon semiconductor layer. However the reference lacks the

unevenness of a surface of said polycrystalline silicon semiconductor layer being within 10% of a thickness of said polycrystalline silicon semiconductor layer, and variations of positions of peaks of depth distributions of concentration of impurities introduced into said polycrystalline silicon semiconductor layer to determine a conductivity type thereof being within 10% of said thickness of said polycrystalline silicon semiconductor layer, said positions of said peaks being with respect to a surface of said substrate.

The primary reference lacks regarding claim 2 the unevenness of said surface of said polycrystalline silicon semiconductor layer and said variations of positions of the peaks of depth distributions of concentration of the impurities are present under said gate insulting film.

The primary reference shows regarding claim 5: A liquid crystal display device provided with a pixel area on a substrate having a plurality of gate lines (see figure 10 and other), a plurality of drain lines 350, a plurality of thin film transistors (shown at the intersection and elsewhere)and a plurality of pixel electrodes P20 (shown in figures 13-14 and elsewhere) corresponding to said plurality of thin film transistors, and a drive circuit area disposed at a periphery of said substrate and having a drive circuit 352 and 364 (described at the bottom of column 10 and elsewhere) for driving said plurality of thin film transistors, said plurality of thin film transistors comprising: a polycrystalline silicon semiconductor layer 13 formed on said substrate 50, a gate electrode 9 formed on said polycrystalline silicon semiconductor layer with a gate insulating film (shown in figures 14b and 14c) interposed therebetween, an insulating film 65 to cover said polycrystalline silicon semiconductor

layer, said gate insulating film and said gate electrode, a drain electrode 72 formed on said insulating film and electrically connected to said polycrystalline silicon semiconductor layer, and a source electrode 71 formed on said insulating film, spaced from said drain electrode and electrically connected to said polycrystalline silicon semiconductor layer.

However, the reference lacks variations of positions of peaks of depth istributions of concentration of impurities introduced into said polycrystalline silicon semiconductor layer to determine a conductivity type thereof being within 10% of said thickness of said polycrystalline silicon semiconductor layer, said positions of said peaks being with respect to a surface of said substrate.

The primary reference lacks regarding claim 6 the variations of positions of the peaks of depth distributions of concentration of the impurities are present under said gate insulating film.

So the two missing element from the claims are the flatness of the layer and the evenness of the doping (the roughness under the gate electrode insulator is inherent as no one gets the roughness down to zero). Regarding the smoothness, the secondary references indicate that keeping the surface smooth improves the device performance. Takahashi et al indicates that the roughness should be kept to a few nm in the abstract, which is less then 10% of the 100nm thickness mentioned in the reference. Hasegawa indices that the surface should be smooth (as possible- abstract, and less than 10 angstroms in spec) and that that enables the ability to control doping depth (col. 6, lines 30-49). Ipri indicates creating a smooth surface is desirable and

that it gives good device properties (abstract). Therefore in the device of Yamazaki it would have been obvious to one of ordinary skill to retain as smooth a surface as possible (including within 10% or better) for the purposes of better device properties as taught in any of the three secondary references.

The smooth surface should enable better control of doping depth, but also Hasegawa indicates discusses it as desirable (in the connection with the discussion of giving even device properties it is described as an end goal). Therefore it would have been inherent to the Yamazaki device as modified above, but also obvious to one of ordinary skill as the it was indicated as desirable.

Response to Arguments

Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection (the Hasagawa reference clarification is being treated as a new ground of rejection).

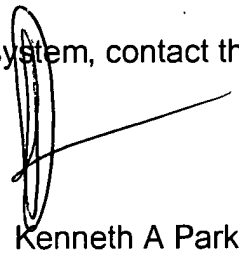
Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth A Parker whose telephone number is 571-272-2298. The examiner can normally be reached on M-F 10:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Kenneth A Parker
Primary Examiner
Art Unit 2871